Bachelor Thesis Review

Faculty of Mathematics and Physics, Charles University

Thesis author	Jan Papesch
Thesis title	RISC–V support in MSIM
Year submitted	2023
Study program	Computer Science
Specialization	Programování a vývoj software
Review author	Filip Kliber — Reviewer
Department	Department of Distributed and Dependable Systems

Overall

	good	OK	poor	insufficient
Assignment difficulty		X		
Assignment fulfilled	X			
Total size *... text and code, overall workload*		X		

The goal of this thesis was to add a support of emulating RISC–V CPU in the context of MSIM emulator used for teaching the Operating Systems course. Author had to study and understand a manual of the RISC–V architecture, which is on its own an intricate task they tackled well. They also needed to understand the architecture of the MSIM emulator, and decouple the implementation of CPU (formerly MIPS R4000) in order to provide a support for simulation of different CPU. Overall, I recommend this thesis for defense.

Thesis Text

	good	OK	poor	insufficient
Form *... language, typography, references*	X			
Structure *... context, goals, analysis, design, evaluation, level of detail*		X		
Problem analysis		X		
Developer documentation		X		
User Documentation		X		

Textual part of the thesis is well-written and well-structured. Author explains both the MSIM simulator and RISC–V architecture enough for the reader to gain necessary background, but without going too much into details. The RISC–V manual itself is more than 200 pages of technical specification, in which the author managed to find all the necessary information to make logical design choices for the implementation.

I think the introduction should explain in greater detail what are the goals of the thesis. For example, it was not clear to me whether the implementation should support a multi-CPU environment or just support different CPUs (the thesis mentioned both scenarios). Also, some of the RISC–V extensions the author presented were not implemented and most likely don't need to be implemented for the purpose of the Operating Systems course. Why are they even mentioned in the first place (e.g. the hypervisor extension)?

Thesis Code

	good	OK	poor	insufficient
Design *... architecture, algorithms, data structures, used technologies*		X		
Implementation *... naming conventions, formatting, comments, testing*	X			
Stability		X		

The implementation consist of modified MSIM simulator that defines a contract for `general_cpu` in order to decouple the notion of CPU from the simulator and provide an interface that can be used when implementing a CPU in the MSIM. The code is well organized and mostly readable. The implementation contains plenty of unit tests as well as some integration/system tests, which indicates the correctness of the implementation. The source code is commented as well, but they do contain quite a lot of typos (i.e. "Rainse an interrupt", "describinfg cpu methods"). Author states that the implementation of Control and Status Registers using an array has "rather large disadvantage of how much space is wasted". The array would only be 16KiB in size, which shouldn't be considered as *too big*. Some form of hash–table could be used as well. Author refactored the original implementation of MIPS CPU in such a way that MSIM supports both CPUs. Is there any plan drop the support for MIPS altogether, since it's discontinued?

Overall grade Excellent

Award level thesis Yes

Date

Signature